


Substitute for Form 1449A/PTO (Modified) (use as many sheets as necessary)				Attorney Docket No.: 04259.P033		Application Number: 09/955,566	
				First Named Inventor: Manish Shah, et al.		RECEIVED MAR 11 2002	
				Filing Date: September 17, 2001		Technology Center 2600	
U.S. PATENT DOCUMENTS							
Exam. Initial*	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	
		Number	Kind Code ² (If known)				
SN		6,148,043		Fujimoto	11/14/2000		
SN		6,141,391		Morelos-Zaragoza, et al.	10/31/2000		
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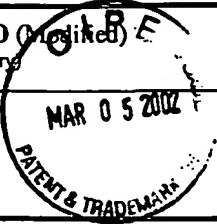
FOREIGN PATENT DOCUMENTS								
Exam. Initial*	Cite No. ¹	Foreign Patent Document			Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD- YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
		Office ³	Number ⁴	Kind Code ⁵ (If known)				

Examiner Signature		Date Considered	6/14/2005
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¹Unique citation designation number. ²See attached Kinds of U.S. Patent Documents. ³Enter Office that issued the document, by the two-letter code (WIPO Standard S.3). ⁴For Japanese patent documents, the indication of the year of reign of the Emperor must precede the serial number of the patent document. ⁵Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁶Applicant is to place a check mark here if English language Translation is attached.

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OTHER ART - NO PATENT LITERATURE DOCUMENTS Technology Center 2600			
Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	Translation ²
SN		JOHN G. PROAKIS, Block and Convolutional Channel Codes, Digital Communications, Fourth Edition, Pages 416 - 547, McGraw-Hill Series in Electrical and Computer Engineering, New York, NY.	
SN		"www.inventra.com/inventra/softcore/workshop/MultiRaFiltDes95/" MENTOR GRAPHICS, Hardware Design of Decimators/Interpolators, Pages 1-38.	
SN		"www.mentor.com/inventra/softcore/workshop/SDmod95/", MENTOR GRAPHICS, Introduction to AD/DA Converters, Pages 1-27.	
SN		http://www.mentor.com/inventra/softcore/workshop/SDHWDdes95/ MENTOR GRAPHICS, Design of the Decimation & Interpolation Filters, Pages 1-57.	
SN		http://www.mentor.com/inventra/softcore/workshop/Applications95/ , MENTOR GRAPHICS, Sigma Delta Converter Applications, Pages 1-5.	

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INFORMATION DISCLOSURE

STATEMENT BY APPLICANT

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Complete if Known

Application Number	09/955,566
Filing Date	September 17, 2001
First Named Inventor:	Manish Shah
Art Unit	2631
Examiner Name	Not Yet Assigned
Attorney Docket Number	004259.P033

Sheet

of

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U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Document Number		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)				
SN		US-	4,015,238	3/29/1977	Robert Curtis Davis	RECEIVED AUG 17 2004 Technology Center 2600
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		US-				
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		Country Code ³	Number ⁴	Kind Code ⁵ (if known)				
SN		WO	00/74264	A1	12/7/2000	Martone, Massimiliano		
SN		WO	01/59937	A2	8/16/2001	Qualcomm Inc.		

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First Named Inventor:

Manish Shah

Art Unit

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Examiner Name

Not Yet Assigned

Attorney Docket Number

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AUG 17 2004

NON PATENT LITERATURE DOCUMENTS

Technology Center 2600

Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T ²
SN		BREE, ET AL., "A Bit-Serial Architecture For A VLSI Viterbi Processor", Communications Systems Research Group, University of Saskatchewan, Saskatoon, IEEE, WESCANEX '88, 1988, pages 72-77.	
SN		BIVER, ET AL., "Architectural Design and Realization Of A Single-Chip Viterbi Decoder", Elsevier Science Publishers B.V., INTEGRATION, The VLSI Journal 8 (1989), October, No. 1, Amsterdam, NL, Pages 3-16.	
SN		BREE, ET AL., "A Modular Bit-Serial Architecture For Large Constraint-Length Viterbi Decoding", Communications Systems Research Group, University of Saskatchewan, Saskatoon, Canada, IEEE International Conference on Communications", 1990, pages 1501-1506.	
SN		CHOI, ET AL., "Viterbi Detector Architecture For High-Speed Optical Storage", 1997, IEEE TENCON - Speech and Image Technologies for Computing and Telecommunications, ASIC Center Corporate Technical Operations SAMSUNG Electronics, Vol. 1, Dec 1997, pages 89-92.	
SN		MARIE-LAURE BOUCHERET, IVAR MORTENSEN and HENRI FAVARO, "Fast Convolution Filter Banks For Satellite Payloads with On-Board Processing," IEEE Journal On Selected Areas In Communications, Vol. 17, No. 2, February 1999	
SN		W.H. YIM and F.P. COAKLEY, "On-Board Processing For KA-Band Applications", University of Surrey, UK, Publication Date, February 11, 1993., XP 000458011, pp. 225-229.	
SN		BOUCHERET/MORTENSEN/FAVARO, "Fast Convolution Filter Banks for Satellite Payloads with On-Board Processing," IEE Journal on Selected Areas in Communications, February 1999, pp. 238-247, Vol. 17, No. 2, XP-000851758	
SN		HASHIDA MITSUYOSHI, "Hierarchical Network Management System and Control Method for Network Management Information," Patent Abstracts of Japan, Publication No. 07226777	

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